An 8-Channel, 46-ps-Precision TDC ASIC with Improved Vernier Delay Loop for STCF EMC*

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An 8-channel Time-to-Digital Converter (TDC) with high precision and high linearity for the electromagnetic calorimeter (EMC) in the super tau-charm facility (STCF) is presented. The 3-level quantization structure is employed in the proposed TDC to achieve high time resolution and wide dynamic range simultaneously. A double-edge-triggered counter characterized with metastability eliminating is used as the first level. The second and third level are implemented with a polyphase clock sampler and a modified Vernier Delay Loop (VDL) with automatic reset mechanism, respectively. Two low-jitter Delay Locked Loops (DLLs) with different length are utilized to assist in vernier measurement and the polyphase clocks are also provided by one of the DLLs. Theoretical analysis with respect to the optimal combination of DLL length and reference clock frequency has been presented. The proposed 8-channel TDC is implemented using 180-nm standard CMOS process with 1.8-V power supply. Under the reference clock frequency of 100-MHz, the TDC is realized with a resolution of 41.7-ps and a dynamic range of 2560-ns. According to testing results, the best single-shoot precision is 46-ps and good consistency among all channels can be observed. The effect of sliding scaled technique on improving conversion linearity is also proved with experiment results. In asynchronous measurements, the maximum differential nonlinearity (DNL) and the integral nonlinearity (INL) are less than 0.4-LSB and 0.5-LSB respectively.

Keywords: STCF, TDC, Vernier, sliding scaled technique, high linearity

I. INTRODUCTION

As the key component of time measurement electronics, Time-to-Digital Converter (TDC) has become a research hotspot in nuclear detection [1, 2] and medical imaging [3]. The super tau-charm facility (STCF), under construction in China, is the new accelerator-based experimental facility with ultra-high luminosity for particle physics [4]. The STCF facility is equipped with multiple detectors, including the electromagnetic calorimeter (EMC) which is used to measure the energy of photons and electrons with high efficiency and high resolution. Besides, a good time resolution for STCF EMC is also required when it comes to background suppression, gamma-neutron discrimination and events identification [5]. The Pure CsI (pCsI) crystal scintillator with an avalanche photodiode (APD) readout is adopted in STCF EMC and the time stamps are acquired through front-end readout circuit (ROC) with leading edge discrimination (LED) and digitized with TDC [6]. The time resolution of full response is supposed to be better than 300-ps for 1 GeV energy deposits, including the optical process and the response of APD and electronics [7]. While the decay time of pCsI used in this experiment can be as large as 30-ns [8], and the large capacitance (270-pF) of the adopted APD detector (Hamamatsu S8664-1010) will cause much input noise to front-end circuit [5]. These two factors will both make it hard to get the time precision of ROC with ultra-high level, for example, a ROC for APD with time precision of 270-ps has been implemented by our team [9]. To realize the target time resolution of 300-ps for electronics, the TDC is expected to reach a resolution of 100-ps.Because an excessive number of readout channels (6732 for the barrel part and 1938 for the endcap part [7]) are expected to be implemented in the detector, the ROC and TDC have been monolithically integrated on an ASIC (application-specific integrated circuit) for high operational efficiency. The aim of this paper is to investigate the TDC ASIC suitable for multi-channel integration, with a resolution of 100-ps or less and high linearity.

Plenty of time-to-digital conversion algorithms and architectures have been proposed over the past few decades. The ASIC based TDC can be divided into three categories [10] – sampling TDC, noise shaping TDC and stochastic TDC. Due to the request for real-time measurement and high counting rate in STCF ECAL, noise shaping TDC which performs with multiple samples to get a high resolution is not applicable. Stochastic TDC is also not suitable in this application scenario for the large die area it occupies [11]. The counter based TDC is the simplest sampling TDC structure which has a scalable dynamic range, but it needs a high-frequency oscillator to realize high resolution (for example, an oscillator with 8 phases and frequency of 3.125-GHz is employed to get a resolution of 40-ps in [12]). The tapped delay line is an ever-popular and easily realized TDC whose resolution is typically limited by the channel length of transistor. The unit delay of such TDC can be relatively fixed with delay locked loop (DLL) [13] or phase locked loop (PLL) [14] to overcome the limitations of process, voltage and temperature (PVT) variations. The front-end circuit is realized using 180-nm CMOS

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process with 3.3-V power supply, so as to obtain better dynamic range and noise performance. As a result, being manufactured with the same process, it's hard to get the propagation delay of a controlled gate lower than 100-ps, so that using only the counter or the delay line cannot achieve our design goals. Pulse shrinking [15] and time amplifying [16] are sampling TDC structures with the sub-gate-delay resolution, both operating with the propagation delay difference between the leading edge (rising edge) and the trailing edge (falling edge) of input pulses. However, the unavoidable mismatch of delay cells in these two TDC structures usually leads to poor consistency across multiple channels. Successive-approximation TDC [17] is an alternative approach for high-resolution TDC, but long conversion time is one of its primary drawbacks. Considering its high resolution, high counting rate and superior multi-channel consistency, the vernier TDC [18–21] appears to be more preferred in real-time measurements. Compared with the vernier delay line TDC, the cyclic vernier TDC holds advantages in terms of area occupation and conversion linearity, while lagging in conversion speed [18]. Nonetheless, the cyclic vernier TDC still capable of reaching relatively high speed (i. e. a conversion rate of 6.67-MS/s was realized in [18]).

To get a high resolution (100-ps) and a large dynamic range (2-μs) simultaneously, the Nutt method [22] was proposed with a counter and two fine time-interpolators. The counter is used to get the number of clock cycles between Start and Stop, and the start and stop interpolator are used to measure the interval between Start/Stop signals and their following first clock rising-edge respectively. Then the measured interval between start and stop signal can be expressed as:

$$T_{IN} = T_{REF} + T_{S1} - T_{S2} \tag{1}$$

where T_{REF}, T_{S1} and T_{S2} denote the measuring results of the counter, the start interpolator and the stop interpolator, respectively. A finer resolution can be realized when the start and stop interpolators are further divided into more measuring levels. Another merit of the Nutt method based TDC is that it naturally implements the sliding scale technique [20], which can greatly improve the measuring linearity of TDC.

To meet the requirements of STCF EMC, an 8-channel, Nutt method based, 3-level TDC is proposed in this paper. The first level is realized with a coarse counter and the second level based on polyphase clock sampler is used to measure the time residue of the first level. The time margin of the second level is quantized with a modified Vernier Delay Loop (VDL) which serves as the finest level of this TDC. The polyphase clocks utilized in the second level are provided by a low-jitter DLL which in company with another shorter DLL, serves for vernier measurements in the finest level.

The rest of this paper is organized as follows. Section II introduces the overall frame work and principles of the proposed TDC, and gives analysis of some key parameters. The circuit design of DLL and 3-level TDC is described in Section III. The experimental setups and measurement results are presented in Section IV. Section V summarizes and concludes this work.

II. FRAMEWORK AND ANALYSIS

A. The Framework and Principles of the Proposed TDC

Fig. 1 shows the overall framework of the proposed TDC and the structure of one channel. The PLL, DLLs and coarse counter are global for the chip and 8 TDC channels with the same structure can operate independently. In actual applications with ROC, one TDC channel is used to sample the external start signal and the trigger signal generated by ROC, also called as the stop signal, is measured by another channel. The time interval between start and stop is calculated and stored off-chip, which is known as the time stamp.

The reference clock of the chip, named as Clk, can be furnished by an integrated PLL or directly from the off-chip clock source. As shown in Fig. 1, DLL-1 and DLL-2 using Clk as the input clock are composed of delay lines with n and n-1 delay cells, respectively. The counter as the first TDC level can be triggered with both rising and falling edges of Clk. The results of the counter are delivered continuously to each TDC channel. The second TDC level is realized with multi-phase clocks produced by DLL-1, which are fed to the clock sampler in each channel. The residual time of the second level, also known as the time interval between the hit event and its subsequent polyphase clock's rising edge, is measured by the third TDC level – a vernier delay loop. The vernier measurement is carried out utilizing the slightly different delay-time between two delay cells, τ_1 and τ_2, which are controlled by DLL-1 and DLL-2, respectively. The resolution of TDC is determined by the third level and represented in (2).

$$\begin{aligned} Re = \tau_2 - \tau_1 &= \frac{1}{(n-1)f_0} - \frac{1}{nf_0} \\ &= \frac{1}{n(n-1)f_0} \end{aligned} \tag{2}$$

where f_0 denotes the frequency of Clk. The dynamic range of TDC proportionates to the number of counter digits, which can be increased according to the limits of power consumption and die area [23]. We can use (3) to signify the dynamic range of this TDC in which N_1 denotes counter digits' number.

$$DR = \frac{2^{N_1}}{f_0} \tag{3}$$

B. Tradeoffs Among Key Parameters

From the formula (2), we can see that the values of n and f_0 are supposed to be increased to get a finer resolution, which means we should insert more delay cells in DLLs or use reference clock of higher frequency. The precision of TDC is mainly up to two components, the quantizing noise and the random noise. The former depends on the value of resolution which can be denoted in time domain as follow [13].

$$\sigma_q = \frac{Re}{2\sqrt{3}} \tag{4}$$

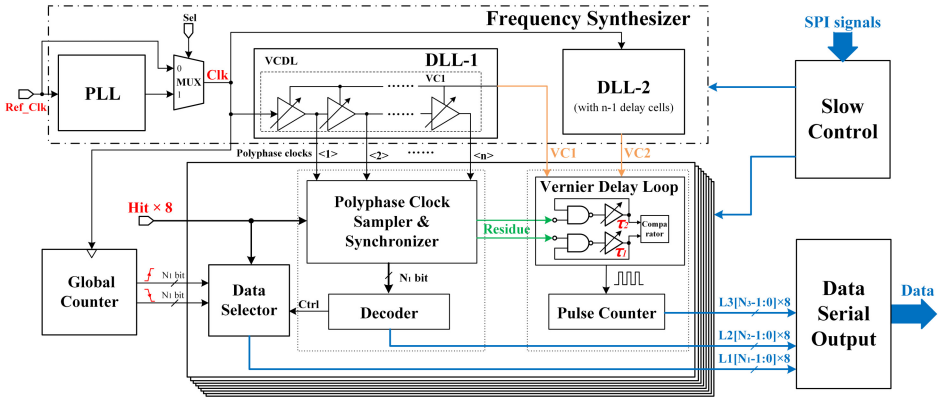

Fig. 1. The structure of the proposed 8-channel TDC.

The jitters generated from the reference clock, the hit signals and produced by DLLs make the precision degenerate likewise, contributing to random noise in phase domain. Assuming the clock and hit signals are as clean as we suppose, the jitter mostly arises from DLLs. Fig. 2(a) shows how the jitter from DLLs affect the precision of TDC. A situation is assumed that the hit signal locates between $Clk < n-1 >$ and $Clk < n >$ provided by DLL-1, so that a replica of $Clk < n >$ is delivered to the VDL for the finest quantization. The jitter generated by a single delay cell can be indicated as σ_0, owing to noises from the control voltage, power supply and substrate. The jitter of $Clk < n >$ is $\sqrt{n}\sigma_0$ which is also the maximum accumulated jitter of DLL-1. As shown in Fig. 2(b), the cycling occurs for m times on loops corresponding to Hit and $Clk < n >$, and $OUTA$ and $OUTB$ are output signals of VDL. On the premise that jitters generated by the 4 cascaded delay cells in VDL are uncorrelated, the accumulated jitters on $OUTA$ and $OUTB$ are represented by (5) and (6), respectively.

$$\sigma_{r1} = \sqrt{4m}\sigma_0 \tag{5}$$

$$\sigma_{r2} = \sqrt{n+4m}\sigma_0 \tag{6}$$

At the end of cycling, $OUTA$ and $OUTB$ are fed to an arbiter for phase comparison. So that the time uncertainty due to jitter can be regarded as the accumulation of σ_{r1} and σ_{r2} and denoted by:

$$\sigma_r = \sqrt{\sigma_{r1}^2 + \sigma_{r2}^2} = \sqrt{n+8m}\sigma_0 \tag{7}$$

While the value of m can be deduced with the relation between τ_1 and Re.

$$m = \frac{\tau_1}{Re} = n-1 \tag{8}$$

The total time uncertainty, or time precision of TDC, is represented by:

$$\sigma_T = \sqrt{\sigma_q^2 + \sigma_r^2} \tag{9}$$

We have designed the delay cell with symmetrical current-starved structure [24] as shown in Fig. 2(c), which is characterized with almost equal rise and fall times. To keep the phase of delay cell not reversed, a delay cell is composed of two current-starved inverter whose propagation delay is controlled by DLL's output voltage ($VC1$ or $VC2$). If we define the toggle point for both rising edge and falling edge as $V_{DD}/2$, the unit propagation delay in DLL-1 can be represented by:

$$\tau_1 = \frac{V_{DD}C_L}{I_{CS}} = \frac{1}{nf_0} \tag{10}$$

where C_L denotes the parasitic capacitance on the output node of every stage, I_{CS} denotes the mean value of charging or discharging current through C_L during output level switching. According to [25], the phase noise of delay cell is dominated by white noise and the low frequency noise can be neglected when the rising edge and falling edge are symmetric. Fig. 2(d) shows the noise model of delay cell considering a positive input step in which the noise contribution of PMOS is omitted. For simplicity, the bias transistors ($NM2$, $PM2$ in Fig. 2(c)) working in triode region are replaced with resistors, on which the voltage drop can be neglected. The input transistor ($NM1$ in Fig. 2(d)) is assumed to be in saturation for simplification. Then the spectral density of output noise [26] can be described by:

$$S_{inN} = \frac{8kT\gamma I_{CS}}{V_{DD} - V_{tN}} + \frac{4kT}{R_D} \tag{11}$$

where V_{tN} is the threshold of NMOS and R_D denotes the value of equivalent resistor of $NM2$ in Fig. 2(c). As R_D can be considered a constant when the bias of $NM2$ is fixed, we adopted the phase noise model for inverter proposed in [27] to get the spectral density of delay:

$$S_{t_d} = \frac{t_d^2}{I_{CS}^2} sinc^2(ft_d) S_{inN} \tag{12}$$

where t_d is the statics of random delay variable and it can be represented by:

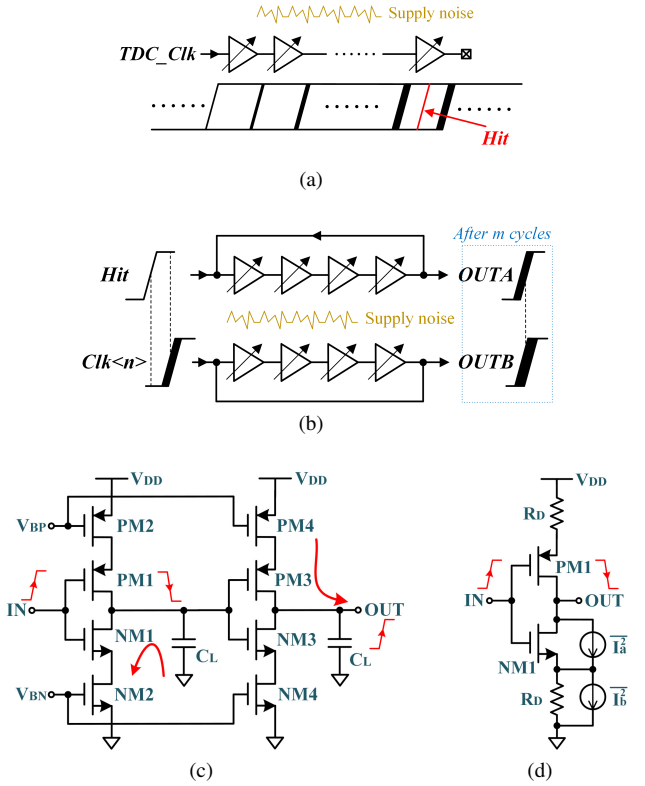

Fig. 2. (a) Jitter accumulations in the second level. (b) Jitter accumulations in the third level. (c)The simplified schematic of delay cell. (d) The noise model of delay cell.

$$t_d = \frac{\tau_1}{2} = \frac{V_{DD}C_L}{2I_{CS}} \tag{13}$$

Then the mean square value of t_d can be deduced with Wiener–Khinchine theorem [27]:

$$\sigma_{t_d}^2 = \int_0^\infty S_{t_d} df = \frac{t_d}{\pi I_{CS}^2} S_{inN} \int_0^\infty sinc^2(x)dx \tag{14}$$

With (10), (11), (12) and (13) this formula can be simplified to:

$$\begin{aligned} \sigma_{t_d}^2 &= \frac{kTV_{DD}C_L}{I_{CS}^3}\left(\frac{2\gamma I_{CS}}{V_{DD}-V_{tN}} + \frac{1}{R_D}\right) \\ &= \frac{kT\left(\frac{2\gamma V_{DD}C_L}{V_{DD}-V_{tN}} + \frac{1}{R_D n f_0}\right)}{(V_{DD}C_L)^2 (nf_0)^2} \end{aligned} \tag{15}$$

On the assumption that the jitters produced with negative input step is equivalent to that with positive input step for a current-starved stage, the jitter of this delay cell with positive input is represented by:

$$\sigma_0^2 = 2\sigma_{t_d}^2 \tag{16}$$

The terms except for n and f_0 in formula (15) can be regard as constants. f_0 is confined within (50-MHz, 100-MHz) in view of power consumption. For simplification, the resolution of TDC is set to a fixed value (e. g. 45-ps). The quantized jitter, σ_q in formula (4), is fixed too. Thus, we just need to reduce the random part of jitter, which is derived from (2), (7), (8), (15) and (16).

$$\sigma_r^2 = \frac{(9n-8)kT\left(\frac{2\gamma V_{DD}C_L}{V_{DD}-V_{tN}} + \frac{(n-1)Re}{R_D}\right)}{(V_{DD}C_L)^2((n-1)Re)^{-2}} \tag{17}$$

With (17), we can understand that to minimize the random jitter as much as possible, it is necessary to use smaller values of n. As Re is fixed at 45-ps, we determine that f_0=100MHz and n=16. As a result, the ideal resolution of the proposed TDC is about 41.7-ps.

III. DESIGN OF CIRCUIT

A. Delay Locked Loop

The structures of the two DLLs integrated in TDC are almost identical, as shown in Fig. 3(a), except for the voltage-controlled delay lines (VCDLs) containing different numbers of delay cells. According to the analysis above, the VCDLs in DLL-1 and DLL-2 contain 16 and 15 cells respectively. The reference clock with a frequency of 100-MHz is fed to DLL-1 and DLL-2 which operate independently and do not need to be synchronized.

The lock controller [28] is used to keep the DLL from false locking and harmonic locking by comparing the first phase and several intermediate phases. The delay of VCDL is forced to range within 8-ns to 13.33-ns when the lock controller is enabled, which can also reduce the time it takes for DLL to get locked. The phase detector operates with the first and the last phase and determines the charging or discharging status of charge pump. The complementary switches, dummy transistors and the wide-swing cascaded current mirror are adopted in the charge pump to improve the matching degree of charging and discharging, thereby a much smaller locked phase error can be realized. Besides, the start-up circuit is used to provide a proper initial value to $VC1$ and $VC2$.

The VCDL is made up of 15/16 cascaded delay cells and 2 dummy cells, which are all based on the modified current-starved structure. As shown in Fig. 3(b), variable PMOS resistances ($PM2$, $PM5$) and variable NMOS resistances ($NM2$, NM) are controlled by V_{BP} and $VC1$ respectively, which vary in opposite directions. With appropriate transistor dimensions, we can get an output with approximately equal rising and falling time across the tuning range. However, the transistor $NM0$ used for biasing can contribute considerable noise, so that only one bias circuit is used in a DLL and the two control voltages, $VC1$ and V_{BP}, are shared by all involved delay cells either in the VCDL or in TDC channels. The constant MOS resistances ($PM3$, $PM6$, $NM3$ and $NM6$) are employed to supply a basic working current and guarantee that the delay cell still works when $VC1$ lower than the threshold voltage of NMOS, which can prevent the DLL from being inactive.

Fig. 3(c) shows the simulated delay-voltage characteristics under different PVT conditions. The effective tuning range

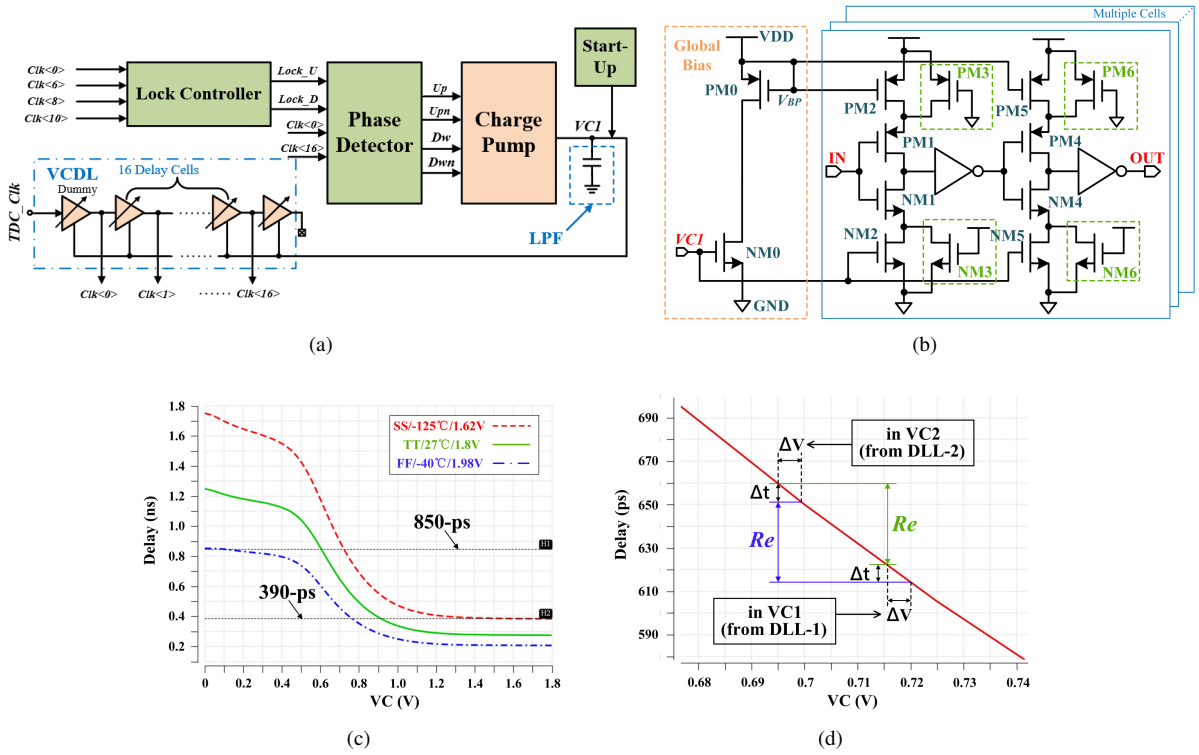

Fig. 3. (a)The structure of DLL-1. (b) The implementation of symmetrical current-starved delay cell. (c) The delay-voltage characteristics of delay cell under different PVT conditions. (d) The effect of the control voltage shift on the TDC resolution.

of this delay cell is 390-ps to 850-ps, which can cover the expected unit-delays for both two DLLs (625-ps for DLL-1 and 666.7-ps for DLL-2). As control voltages are transferred to multiple channels with separate distances to the DLLs, the control voltages shift variously at each channel. As shown in Fig. 3(d), we suppose that the shifts of VC1 given by DLL-1 and VC2 given by DLL-2 are both ΔV. Thanks to the high linearity of delay-voltage characteristic within a small voltage range, the unit delays controlled by VC1 and VC2 are both skewed by Δt. Therefore, the resolutions of all the channels can be considered to be roughly consistent as they are dominated by the difference of those two unit-delays.

B. The First and Second Level

The first TDC level is based on an 8-bit global counter with double-edge-triggered structure [29] shown in Fig. 4(a). The counting results, $CntP$ and $CntN$ obtained with the rising and falling edges of Clk respectively, are delivered to each channel simultaneously. The data selector in channel is used to capture the proper counting result whenever the asynchronous Hit signal arrives, according to the result of the second level, $L2[3:0]$ as shown in Fig. 4(b). If the asynchronous input signal denoted by Hit locates in the first half of clock cycle, we can get $L2[3]=1$ and CntN is chosen as the result of first level. In the case Hit locates in the second half of clock cycle, $CntP$ is chosen. The implementation of double-edge-triggered counter and appropriate settings are aimed to eliminate the metastability of counter.

One of the tasks of the second level is to measure the time interval between Hit and the first rising edge of Clk following Hit, which can be realized with the polyphase clock sampler composed of 16 arbiters, as shown in Fig. 4(b). Another task is to transfer the residual time to the next level with the synchronizer. For example, if $Clk<1>$ is captured by the sampler, the residual time is the time elapsed between Hit and $Clk<1>$. Even though well-matched loads are inserted on both signal paths of the synchronizer, there are still errors between input intervals and output intervals. The maximum error is about 5.1-ps according to Mont Carlo simulation, which can be tolerated as the final resolution is much larger than the error.

C. The Third Level–Vernier Delay Loop

The Vernier Delay Loop (VDL) used to quantize the residual time of the second level is a modified version of that proposed in [18], as shown in Fig. 4(c). There are 2 structurally identical loops in this VDL. The loop with the input named SI_1 is the slow loop and that with the input named SI_2 is the fast loop. SI_1 and SI_2 are exactly the two outputs of synchronizer as shown in Fig. 4(b). SI_1 is supposed to precede SI_2 and the interval between them denoted as T_f varies within 0 ˜625-ps. The edge detect circuit is used to generate a

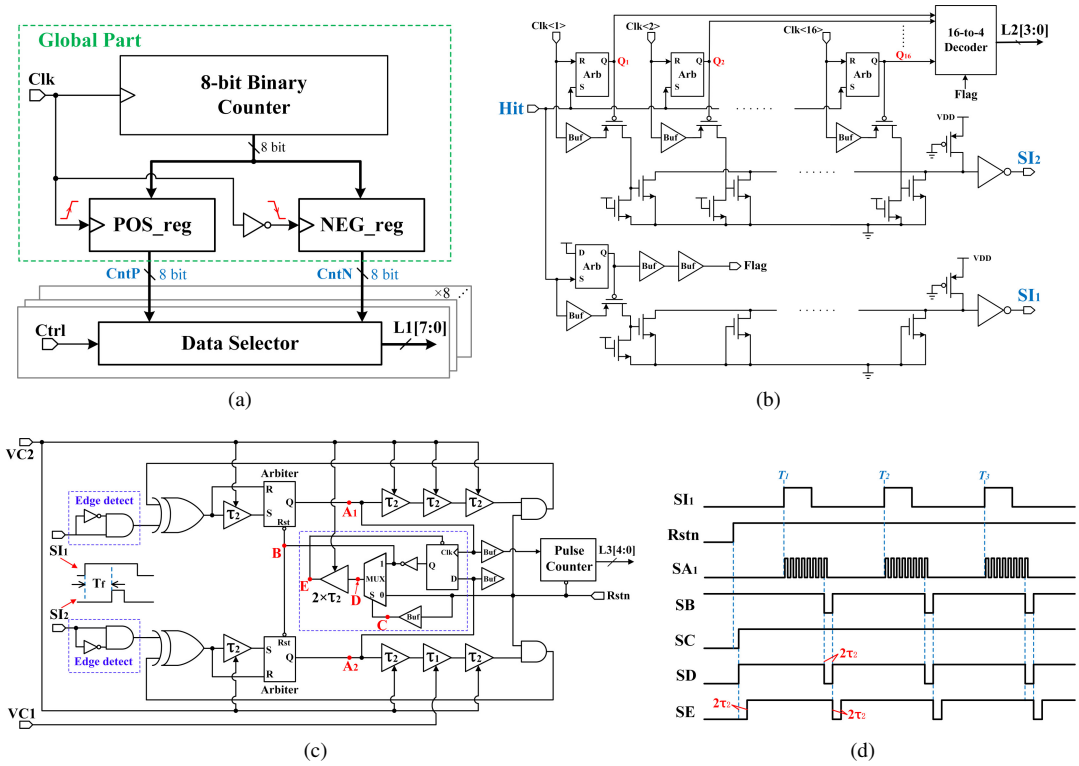

Fig. 4. (a) The structure of double-edge-triggered counter. (b) The schematic of polyphase clock sampler and synchronizer. (c) The schematic of the modified VDL. (d) The timing diagram to illustrate the proposed automatic reset mechanism for VDL.

narrow pulse when the rising edge of SI_1/SI_2 arrives. There are 2 kinds of unit-delays in each loop, namely τ_1 and τ_2 , which are regulated by the control voltages provided by DLL-1 and DLL-2, respectively. The single delay cell and arbiter are used to convert the narrow pulse to a pulse with width of τ_2. The cycle periods are determined by the 3-cascaded delay cells in the scenario that the delays of other logics on the loop can be neglected, which are $3\tau_2$ for the slow loop and $\tau_1 + 2\tau_2$ for the fast loop. As shown in Fig. 4(c), signals at nodes A_1 and A_2 are denoted as SA_1 and SA_2, respectively. SA_1 precedes signal SA_2 by T_f before cycling, and the interval between SA_1 and SA_2 is decreased by $(\tau_2 - 2\tau_1)$ after each cycle. The cycling is stopped when SA_2 catches up with SA_1. The number of cycles it takes to get SA_1 and SA_2 aligned can be obtained with the pulse counter and represented by:

$$n_f = \lceil \frac{T_f}{\tau_2 - \tau_2} \rceil \tag{18}$$

Ideally, the maximum n_f is 15, for which a 4-bit counter is enough. However, in order to calibrate the measurement results, a redundant bit is added.

As the VDL is expected to measure arrival times of sequential pulse, an auxiliary circuit which can make VDL automatically reset after quantization has been realized as shown in the dotted box of Fig. 4(c), where signals at nodes B, C, D and E are denoted as SB, SC, SD and SE, respectively. The timing diagram of critical signals is shown in Fig. 4(d). Before quantization, the global $Rstn$ firstly takes SB to 0 to clear all nodes on the loop and then SB is pull up to 1 to get the loop ready for cycling. The cycling stage of VDL begins as soon as SI_1/SI_2 arrives. When SA_1 and SA_2 are aligned after several cycles, the flip-flop samples to 1 and then SB is taken to 0 and both two loops are cleared. Synchronized with SB, SD and SE are successively pull down to 0 with a delay of $2\tau_2$. Then the flip-flop is cleared and SB, SD, SE are pulled up to 1 in turn. After these steps, the VDL is once again ready for the next quantization. With this automatic reset mechanism, the maximum dead time of VDL is less than 45-ns, which means that the conversion rate of single channel can reach up to 22.2-MS/s. Considering the integration and serial readout of data from 8 channels, the overall conversion rate of the proposed TDC chip can reach 5-MS/s. Along with a fast ROC, the pileup effect in STCF EMC can be mitigated in view of that the background counting rate is 1-MHz [7].

IV. ASIC PROTOTYPE AND PERFORMANCE

A. ASIC Prototype and Experiment Setups

The proposed 8-channel TDC has been taped out using standard 180-nm CMOS process with 1.8-V power supply and the microphotograph of chip is shown in Fig. 5(a). The layout of TDC channel is designed with a strip shape and 8 channels are arranged in a column, which makes $VC1$ and

$VC2$'s distribution paths as short as possible. The chip has a die-area of 1.55-mm $\times$ 1.42-mm, including the pad ring.

Fig. 5(b) shows the experiment setup composed of an oscilloscope to observe signal series, a spectrum analyzer for jitter measuring, 2 pulse generators to provide reference clock and input signals of TDC, a FPGA board and an upper computer for chip controlling, and a logic analyzer used to collect and process measured data. We adopt a clock generator chip, AD9552, to provide the 100-MHz reference clock with jitter below 1-ps, rms. While the reference clock is directly given by pulse generator in linearity evaluation.

B. Performance of DLL

There are three chips that have been tested and verified, named chip-1, chip-2, and chip-3. Unless specifically indicated, all the following measurements are performed with chip-2. Two approaches were adopted to get the jitter of DLL, one is to obtain the phase noise curve of the last polyphase clock and integrate it within frequency shift range of (10 kHz, 20 MHz), the other is to measure jitter directly with the oscilloscope. The jitter of 5-ps, rms can be got with both approaches, which is much less than the resolution of TDC. Other performances are shown in Table. 1.

TABLE 1. The performance of DLLs with 100-MHz reference clock.

Intex	DLL-1	DLL-2
Jitter of the last phase (ps, rms)	5.2	5.1
Duty cycle of the last phase	55%	54%
Locked error (ps)	29.9	35.4

C. Performance of TDC

For the first, we need to determine the actual resolution (LSB) of each TDC channel. As the bin distributions are nearly consistent over all clock periods [29], we just have to evaluate the actual LSB within one clock period. One channel of the pulse generator is dedicated to providing the 100-MHz reference clock, and the TDC input with a frequency of 4.00001-MHz is derived from another channel. In this way, the interval between TDC input and the rising edge of reference clock increases by 0.625-ps with each clock cycle. This interval will cyclically repeat within the range of 0 to 10-ns, which can be considered as an approximate method for code density testing [30].

In ideal scenarios, the number of bins within the 10-ns measuring range is fixed (approximately 240), with an LSB size of around 41.7-ps. However, plenty of non-ideal factors can cause the actual LSB being either larger or smaller. The tested DNL and INL of the second TDC level across 8 channels with high consistency are shown in Fig. 6(a) and Fig. 6(b) respectively. The non-linearity of the second level is mainly arise from mismatches of VCDL in DLL-1, which results in variable "margins" between the second level and the third level. To explain it, we assume 2 kinds of step sizes of the second level with 600-ps and 650-ps, which are also intervals to be measured with VDL. With no considering about non-ideal factors in VDL, the resolution is fixed to 41.7-ps. Then sizes of VDL's last bins for input intervals of 600-ps and 650-ps are set to 16.2-ps and 24.5-ps respectively.

To prevent the last bin within the VDL quantization range from being too narrow to worsen DNL, a bin-size filtration mechanism has been implemented. Firstly, the approximate magnitude of LSB is ascertained. If the size of last bin is less than LSB/4, We combine the last bin with the second-to-last bin into a new bin. Otherwise, the last bin is retained. The bin distribution of Channel-1 within one clock period is shown in Fig. 6(c). After the above processing, the LSBs of eight channels are shown in Fig. 6(d) where we can get approximate measured results across 3 chips. The LSB of channel-1 is larger than that of other channels, which can be explained by the significant deviation of supply voltage in this channel.

TABLE 2. The linearity performance of 8 individual channels.

Channel number	DNL (LSB)		INL (LSB)	
Ch-1	-0.64	0.28	-0.99	1.40
Ch-2	-0.66	0.44	-2.46	1.23
Ch-3	-0.68	0.60	-2.28	0.44
Ch-4	-0.71	0.48	-1.96	2.19
Ch-5	-0.73	0.83	-4.40	5.14
Ch-6	-0.70	0.47	-2.83	1.46
Ch-7	-0.66	0.58	-4.71	2.24
Ch-8	-0.54	0.67	-3.31	2.64

TABLE 3. The linearity performance of different combinations of Start channel and Stop channel.

Start vs Stop	DNL (LSB)		INL (LSB)	
Ch-1 vs Ch-2	-0.24	0.36	-0.45	0.24
Ch-1 vs Ch-3	-0.35	0.37	-0.22	0.49
Ch-1 vs Ch-4	-0.20	0.32	-0.15	0.44
Ch-1 vs Ch-5	-0.26	0.27	-0.23	0.48
Ch-1 vs Ch-6	-0.21	0.25	-0.25	0.38
Ch-1 vs Ch-7	-0.23	0.38	-0.31	0.34
Ch-1 vs Ch-8	-0.24	0.30	-0.33	0.50

The distribution ranges of DNL and INL in each of the 8 channels over one clock period (10-ns) have been shown in Table. 2. We also assessed the linearity in asynchronous measurement mode, wherein Ch-1 serves as the start channel, and one of other channels serves as the stop channel. The code density test was performed again in which Start and Stop are provided by one pulse generator with frequencies of 4.00001-MHz and 4-MHz respectively. Since only measurement results of the second and third levels are collected, the interval between Start and Stop can be considered as randomly distributed within (0, 10 ns) with a 100-MHz reference clock.

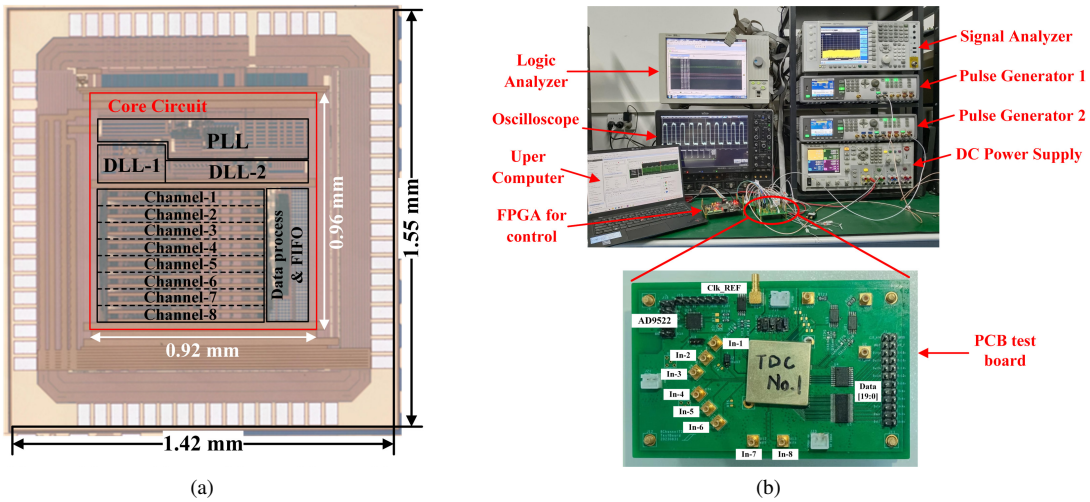

Fig. 5. (a) The microphotograph of the proposed TDC chip. (b) The test system and PCB board for testing.

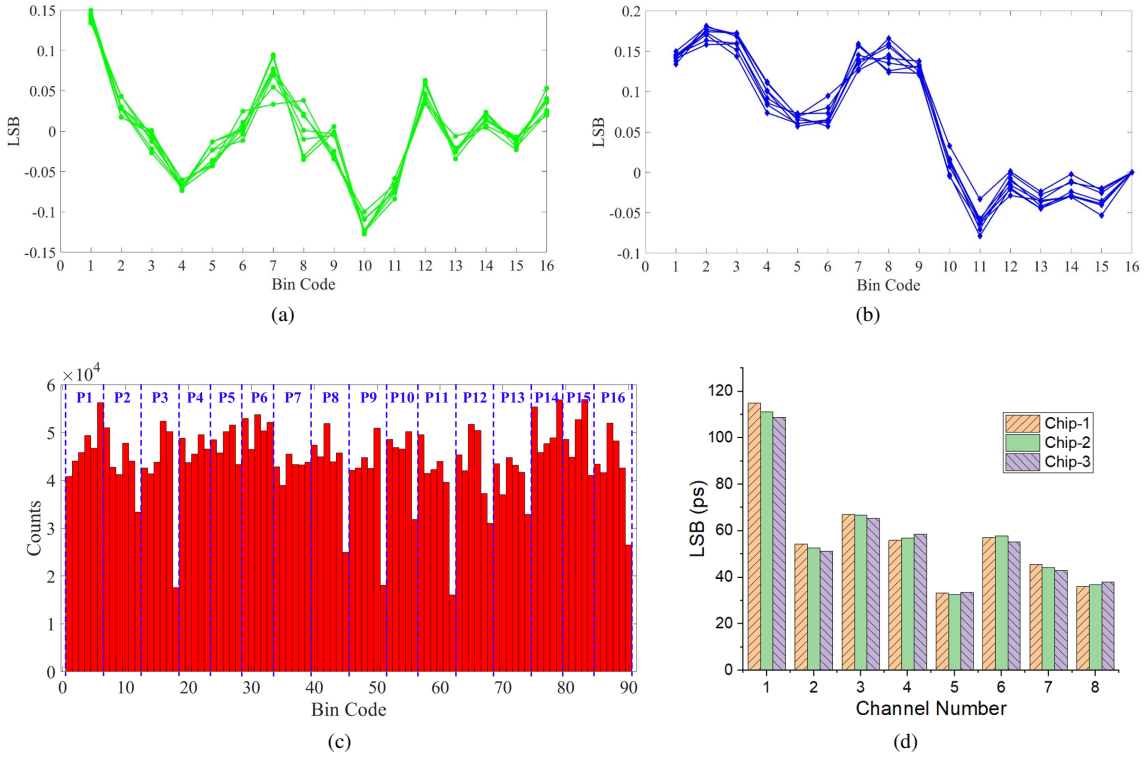

Fig. 6. The test results of (a) DNL and (b) INL across 8 channels, only considering the second level.(The bin code on the x-axis also represents the interval between two adjacent multiphase clocks.) (c)The bin distribution of channel-1 within a measuring range of 10-ns. (d)The actual LSBs of 8 channels across 3 chips.

Table. 3 shows the linearity performance of 7 channel combinations in which we can see DNLs better than 0.4-LSB and INLs better than 0.5-LSB for all test cases. By comparing test results of single-channel and dual-channel, it is convinced that the asynchronous TDC inherently employing the sliding scaled technique provides a great advantage in terms of linearity.

The Single Shoot Precision (SSP) of TDC has been measured with asynchronous mode. The output of pulse generator is divided into two identical signals with a power splitter. One is transmitted to the start channel (Ch-1) through a 0.1-m cable, the other is transmitted to the stop channel (one of other channels) through a 0.3-m cable, which is called as Cable Delay Measurement Test [29]. The best uncalibrated SSP

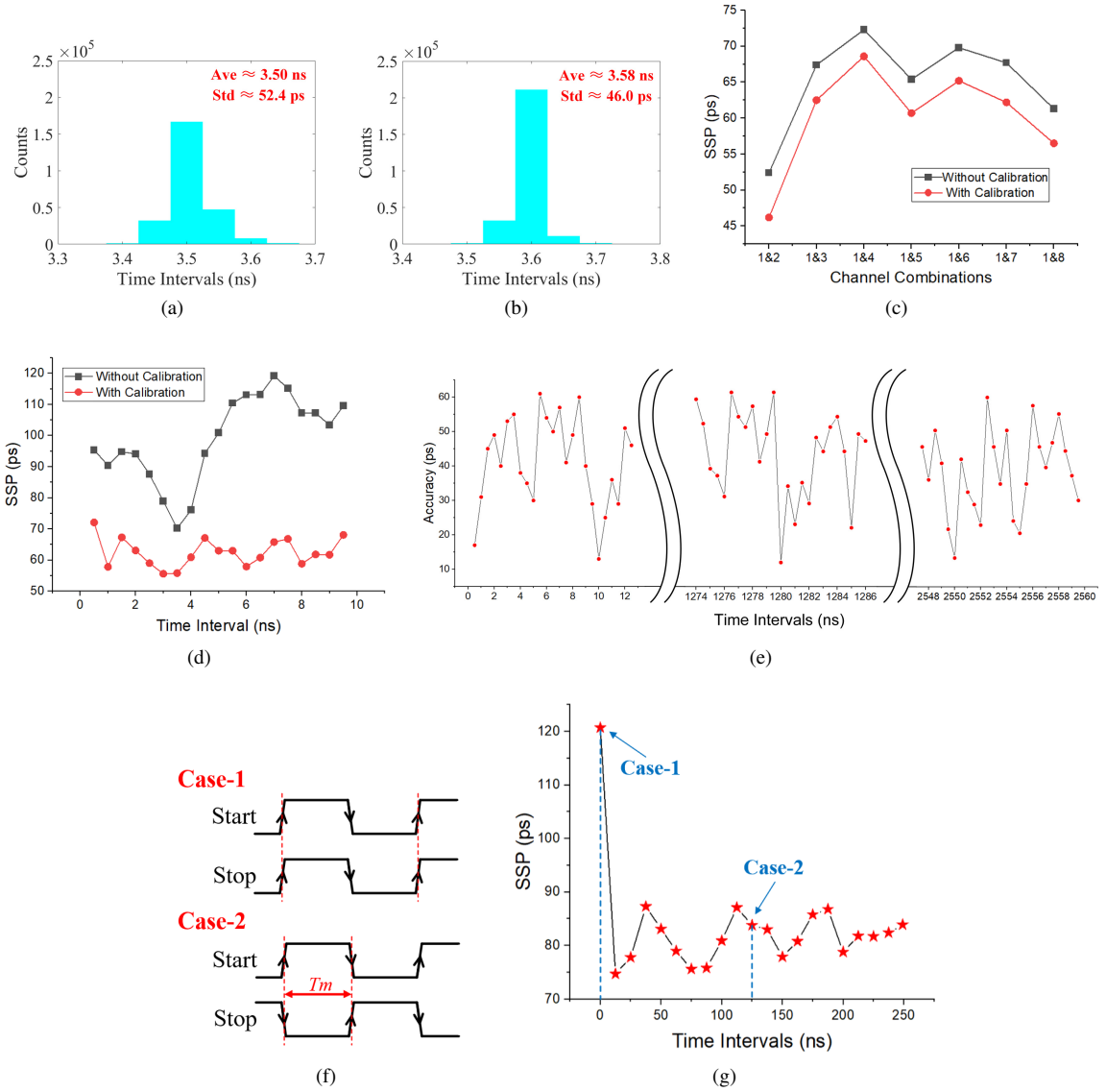

Fig. 7. (a) The uncalibrated SSP and (b) the calibrated SSP with the combination of Ch-1 and Ch-2. (c) The SSP results across 7 channel combinations with cable delay measurement test. (d) The SSP results along the range of (0.5-ns, 10-ns) with the combination of Ch-1 and Ch-2. (e) The tested accuracy along TDC's dynamic range with the combination of Ch-1 and Ch-2. (f) The specification of two cases of correlated cross-talk between Start and Stop. (g) The measured SSP curve with time intervals within (0, 249-ns), which includes the two cases of correlated cross-talk.

of 52.4-ps can be get with the combination of Ch-1 and Ch-2 as shown in Fig. 7(a). The precision can be improved with the look-up table for INL [31]. The principle of calibration is shown below:

$$TDC_{CAL} = TDC_{RAW} + INL[TDC_{RAW}] \tag{19}$$

where TDC_{RAW} and TDC_{CAL} denote raw and calibrated TDC digits respectively. A calibrated SSP of 46-ps can be noticed from Fig. 7(b). The tested SSPs with other channel combinations are shown in Fig. 7(c), which are all in the range of 45-ps to 70-ps after calibration.

To validate the effectiveness of calibration, we measured SSP along an input interval range of (0.5-ns, 10-ns). As shown in Fig. 7(d), SSP results with different inputs become more consistent after calibration. As this calibration method relying on INL results is designed to compensate for non-uniform LSBs, the test results can mutually corroborate with this theory. Hence, the test and calibration method we employed can be proved to be correct. The accuracy representing the error between input and output, is also measured over the dynamic range of TDC as shown in Fig. 7(e). As the metastability has been eliminated with the double-edge-triggered counter, no significant deviation of accuracy was observed in test results.

The precision of TDC can be degraded due to the effect of cross-talk, with which there will be distortion of edges

of Start or Stop. The correlated cross-talk and uncorrelated cross-talk are the two types of mechanism. The uncorrelated cross-talk is usually hard to evaluate and we paid more attention to the correlated cross-talk [32]. An experiment to study the effect of cross-talk has been done. Two adjacent channels, channel-1 and channel-2, are used to get the timestamps of the Start signal and Stop signal respectively. The input pads of these two channels are close to each other, so that the effect of cross-talk on them can be more significant. The frequency of Start and Stop are both 4-MHz and the time intervals between them (denoted as T_m) are varied within (0, 249-ns). As shown in Fig. 7(f), the rising edges of Start and Stop are distorted by each other with T_m = 0, and the rising edge of Stop will be distorted by the falling edges of Start with T_m = 125-ns. The SSP evaluations with variable time intervals have been taken. We can see that in Fig. 7(g) that the SSP with T_m = 0 is significantly worse than other cases, but it is not significant with the case of T_m = 125-ns. It is speculated that this may be because the effect of cross-talk is greater when the rising edges of Start and Stop are coincident. Due to the asynchronous measurement mechanism and the double-edge-triggered counter of this TDC, the effect of metastability can be neglected and the degradation of SSP can be explained with cross-talk. Therefore, these instances with correlated cross-talk should be excluded in the system's operating mode of TDC.

Table. 4 shows the comparison of the proposed TDC with others, which are all suitable for the multi-channel applications. Compared with the Delay Line structure in [33] and the counter structure in [36], the proposed TDC has an advantage in terms of precision. In contrast to the structures based on ring oscillator in [34] and [37], our design exhibits superior conversion linearity. The TDC proposed by [35] is also based on the vernier controlled with dual DLLs, while it has a worse linearity and a slower conversion rate compared to our TDC. [38] and [39] are two TDCs based on Xilinx 7-series 28-nm FPGA, and the performance of our TDC is still competitive among them.

V. SUMMARY

The design of an 8-channel, high precision TDC ASIC for STCF EMC and the experimental results are presented in this work. The proposed TDC is realized with a 3-level Nutt structure, which can reach a wide dynamic range and a high resolution. The sliding scaled technique is employed with the proposed TDC and its role in improving conversion linearity is proved. The prototype chip has been implemented with standard 180-nm CMOS process with a die area of 1.55-mm $\times$ 1.42-mm. According to testing results, the proposed TDC features with a single-shoot precision of 46-ps for the best channel, the DNL better than 0.4-LSB and INL better than 0.5-LSB and good consistency among all channels can be observed. Besides, good consistency in performance across all TDC channels is demonstrated. In view of the flexible vernier-type framework this chip employed, our next step is to further improve the TDC's resolution and expand it to accommodate more channels. The synchronization and matching among multi-channels, the suppression of jitter, as well as temperature compensation techniques will also be investigated in the future work.

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TABLE 4. Comparison of multi-channel TDCs.

Parameters	[33]	[34]	[35]	[36]	[37]	[38]	[39]	This work
Process (nm)	130	350	65	110	180	28	28	180
Type	Delay line	GRO∗	Vernier	Counter	VCRO∗	RO	Counter	Vernier
Channels	1024	48	2	17	1024	/	64	8
Dynamic range (ns)	100	51.8	2500	3400	2100	30	/	2560
SSP (ps)	78.5	93.2	27.6	104	62.1	20	96.8	46.0
DNL/INL (LSB)	0.4/1.2	2.0/2.4	1.7/2.8	0.3/2.5	0.5/2.2	0.7/1.0	0.2/0.3	0.4/0.5
Conversion Rate (MS/s)	500	40	1	/	/	17.2	/	22.2
Power (mW)∗∗	90	/	51.4	188.8	>1200	/	/	93.6∗ ∗ ∗

∗ GRO is the acronym of Gated Ring Oscillator and VCRO represents Voltage Controlled Ring Oscillator.
∗∗ The power consumptions of all TDC channels are included.
∗∗∗ The presented power dissipation of proposed chip is obtained with the conversion rate of 4-MS/s.

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